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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Lukas P.P.P. van Ginneken
Title: Timing Closure Methodology

Application No.: 10/828,547 Filing Date: April 19, 2004
Examiner: Siek, Vuthe Group Art Unit: 2825
Docket No.: MDAI.001US3 Conf. No.: 3884

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Pursuant to 37 C.F.R. §§ 1.56, 1.97 and 1.98, Applicant calls the documents listed on the enclosed Form PTO-1449 to the Examiner's attention in this patent application. Copies of the documents listed on the accompanying Form PTO-1449 are enclosed.

Citation of these documents shall not be construed as (1) an admission that the documents are prior art with respect to the invention or inventions claimed in this application, (2) a representation that a search has been made (other than as indicated by any cited document), or (3) an admission that the cited information is, or is considered to be, material to patentability as defined in § 1.56(b).

Attorney Docket No.: MDAI.001US3
Express Mail No.: EV357277939US

Application No.: 10/828,547

This information disclosure statement is submitted under 37 C.F.R. § 1.97(b) and consequently no fee should be required. The Commissioner is authorized, however, to charge any fee that may be required, or to credit any overpayment, against Deposit Account No. 502664. This form is being submitted in duplicate.

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LABEL NO:**
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Respectfully submitted,



James S. Hsue

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August 31, 2005

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Express Mail No.: EV357277939US

Application No.: 10/828,547

Form PTO-1449 <i>(Substitute)</i>	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	Attorney Docket Number MDAI.001US3	Application/Patent Number 10/828,547
INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use several sheets if necessary)</i>		Applicant/Patent Owner Lukas P.P.P. van Ginneken	
		Filing/Issue Date April 19, 2004	Group Art Unit 2825

U.S. PATENTS

Examiner Initial		Patent Number	Issue Date	First Named Inventor	Class	Subclass	Filing Date

U.S. PATENT PUBLICATIONS

Examiner Initial		Patent Application Publication Number	Publication Date	Applicant
PENDING U.S. PATENT APPLICATIONS				

Examiner Initial		Application Number	Filing Date	First Named Inventor	Petition to Expunge? Yes No
FOREIGN PATENT DOCUMENTS					

Examiner Initial		Document Number	Publication Date	Country	Class	Subclass	Translation Yes No
OTHER DOCUMENTS (Include author (if any), title, publisher and place of publication, date and pertinent pages)							

Examiner Initial	Author	Title	Publication	Date
	Alpert, C. and A. Devgan [‘Alpert 1997A’]	"Wire Segmenting for Improved Buffer Insertion"	34th Design Automation Conference (DAC '97) Anaheim, California	June 1997
	Camposano, Raul	“The Quarter Micron Challenge: Integrating Physical and Logic Design”	ISPD '97	1997

	Chan, Vi Cuong and David M. Lewis [“Chan 1996”]	"Area-Speed Tradeoffs for Hierarchical Field- Programmable Gate Arrays"	<i>ACM Symposium</i>	1996
	Chang, Shih-Chieh, Lukas P. P. P. van Ginneken and Malgorzata Marek- Sadowska [“Chang 1996”]	“Fast Boolean Optimization by Rewiring”	International Conference on Computer-Aided Design, 1996 (ICCAD '96), San Jose, CA	November 10- 14, 1996
	Chang, Shih-Chieh	“Layout Driven Logic Synthesis for FPGAs”	<i>31ST ACM/IEEE Design Automation Conference</i>	1994
	Chen, Guangqiu	“An Iterative Gate Sizing Approach with Accurate Delay Evaluation”	<i>Department of Electronics and Communication, Kyoto University</i>	
	Chen, Wei	“Gate Sizing with Controlled Displacement”	<i>Department of Electrical Engineering –System University of Southern California, Los Angeles</i>	
	Chen, Wei	“Simultaneous Gate Sizing and Placement”	<i>Department of Electrical Engineering – System University of Southern California, Los Angeles</i>	
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	Cong, Jason, Cheng-Kok Koh and Kwong-Shing Leung [“Cong 1996A”]	"Simultaneous Buffer and Wire Sizing for Performance and Power Optimization"	ISLPED	1996

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	Dunlop, A. E., V. D. Agrawal, D. N. Deutsch, M. F. Juki, P. Kozak, and M. Wiesel [“Dunlop 1984”]	“Chip Layout Optimization Using Critical Path Weighting”	<i>21st Design Automation Conference</i>	1984
	Grodstein, Joel, Eric Lehman, Heather Harkness, Bill Grundmann and Yosinotori Watanabe [“Grodstein 1995”]	“A Delay Model for Logic Synthesis of Continuously-Sized Networks”	<i>International Conference on Computer-Aided Design (ICCAD '95)</i> <i>San Jose, California</i>	November 5-9, 1995
	Hojat, S. and P. Villanubia. [“Hojat 1997”]	“An Integrated Placement and Synthesis Approach for Timing Closure of Power PC Microprocessors”	<i>1997 International Conference on Computer Design (ICCD '97)</i> <i>Austin, Texas</i>	October 12-15, 1997
	Jiang, Yi-Min	“Post-Layout Logic Restructuring for Performance Optimization”	<i>34th Design Automation Conference</i>	1997
	Kannan, Lalgudi	“A Methodology and Algorithms for Post-Placement Delay Optimization”	<i>31st ACM/IEEE Design Automation Conference</i>	1994
	Keutzer, Kurt	“The Future of Logic Synthesis and Physical Design in Deep-Submicron Process Geometries”	<i>ISPD '97</i>	1997

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	Lou, Jinan	“Concurrent Logic Restructuring and Placement for Timing Closure”	<i>Department of Electrical Engineering – Systems University of Southern California, Los Angeles</i>	
	Mains, Robert E., Thomas A. Mosher, Lukas P. P. P. van Ginneken and Robert G. Damiano [“Mains 1994A”]	“Timing Verification and Optimization for the PowerPC Processor Family”	<i>Proceedings, IEEE International Conference on Computer Design: VLSI in Computers and Processors, 1994 (ICCD '94)</i>	October 10-12, 1994
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	Murofushi, Masako	“Layout Driven Re- Synthesis for Low Power Consumption LSI’s”	<i>34th Design Automation Conference</i>	1997
	Neumann, Ingmar	“Cell Replication and Redundancy Elimination During Placement for Cycle Time Optimization”	<i>IEEE</i>	1999
	Otten, Ralph H. J. M. [“Otten 2000”]	“A Design Flow for Performance Planning: New Paradigms for Iteration Free Synthesis”	<i>Architecture Design and Validation Methods</i> (Egon Borger, Ed.)	2000 (Springer-Verlag New York, Inc.)
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	Pedram, Massoud and Bryan Preas [“Pedram 1989”]	“Interconnection Length Estimation for Optimized Standard Cell Layout”	<i>International Conference on Computer Aided Design</i>	1989
	Pedram, Massoud	“Logical-Physical Co-Design for Deep Submicron Circuits: Challenges and Solutions”	<i>Department of Electrical Engineering – Systems University of Southern California</i>	
	Pedram, Massoud	“Panel: Physical Design and Synthesis Merge or Die!”		
	Preas, Bryan T. and Michael J. Lorenzetti (Editors) [“Preas 1988”]	---	<i>Physical Design Automation of VLSI Systems</i>	1988 (© The Benjamin/Cummings Publishing Company, Inc.)
	Rabaey, Jan M. [“Rabaey 1996”]	---	<i>Digital Integrated Circuits: A Design Perspective</i>	1996 (©Prentice Hall)
	Sarabi, Andisheh	“A Comprehensive Approach to Logic Synthesis and Physical Design for Two-Dimensional Logic Arrays”	<i>31st ACM/IEEE Design Automation Conference</i>	1994
	Sarrafzadeh, Majid and C. K. Wong [“Sarrafzadeh 1996”]	---	<i>An Introduction to VLSI Physical Design</i>	1996 (© McGraw-Hill)
	Sato, Koichi	“Post-Layout Optimization for Deep Submicron Design”	<i>33rd Design Automation Conference</i>	1996
	Shah, Jatan	“Wiresizing with Buffer Placement and Sizing for Power-Delay Tradeoffs”	<i>Department of Electrical and Computer Engineering Iowa State University</i>	

	Singh, Kanwar Jit and Alberto Sangiovanni- Vincentelli [“Singh 1990”]	“A Heuristic Algorithm for the Fanout Problem”	<i>27th Design Automation Conference</i>	1990
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	Stok, Leon	“BooleDozer: Logic Synthesis for ASICs”	<i>IBM</i>	1996
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	Vaishnav, Hirendu	“Minimizing the Routing Cost During Logic Extraction”	<i>32nd ACM/IEEE Design Automation Conference</i>	1995
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	van Ginneken, Lukas P. P. P. [“van Ginneken 1990A”]	“Buffer Placement in Distributed RC-tree Networks for Minimal Elmore Delay”	International Symposium on Circuits and Systems, 1990	May 1-3, 1990
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	United States District Court for the Northern District of California	Amended Order RE: Claim Construction of United States Patent Nos. 6,453,446, 6,725,438 and 6,378,114		August 23, 2005
Examiner		Date Considered		
<p>*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.</p> <p>*1 = Copy not submitted because it was submitted in prior application SN / , filed , 20 , relied on under 35 USC §120. *2 = Copy not submitted because it was submitted in prior application SN / , filed , 20 , relied on under 35 USC §120.</p>				

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